

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-23 (Canceled)

Claim 24 (New): A communication terminal comprising:

- a first data bus;
- a second data bus;
- a bus buffer circuit connected to said first and second data buses and having a memory for temporarily storing input data;
- a shift register connected to an external unit;
- a FIFO controller connected to said second data bus and comprising a transmission controller and a reception controller,
 - said transmission controller comprising a first write pointer controller which outputs a first write count signal and a first read pointer controller which outputs a first read count signal,
 - said reception controller comprising a second write pointer controller which outputs a second write count signal and a second read pointer controller which outputs

a second read count signal;

a trigger detector connected to said second data bus and comprising a transmission trigger detector and a reception trigger detector,

said transmission trigger detector counting an input of the first read count signal to generate a first count value, and outputting a first interrupt output control signal when the first count value is equal to a first predetermined value indicating a remaining data amount,

said reception trigger detector counting an input of the second read count signal to generate a second count value, and outputting a second interrupt output control signal when the second count value is equal to a second predetermined value indicating a remaining data amount;

a transmission FIFO circuit connected to said second data bus for storing first data input from said bus buffer circuit according to a first write pointer designating an address where the first data are to be written into, said transmission FIFO circuit reading out the stored first data according to a first read pointer designating an address where the first data are stored;

a reception FIFO circuit connected to said second data bus and said shift register for storing second data input from said shift register according to a second write pointer designating an address where the second data are to be written into, said reception FIFO circuit reading out the stored second data according to a second read pointer designating an address where the second data are stored;

an internal interrupt circuit connected to said second data bus for outputting a first internal interrupt signal, when the first interrupt output control signal is input thereto;

an interrupt circuit connected to said first data bus for generating a first interrupt signal in response to the first internal interrupt signal; and

a central processor letting the data stored in said bus buffer circuit be written into said transmission FIFO circuit, when the first interrupt signal is input thereto.

Claim 25 (New): The communication terminal in accordance with claim 24, wherein said internal interrupt circuit outputs a second internal interrupt signal, when the second interrupt output control signal is input thereto,

said interrupt circuit generating a second interrupt signal in response to the second internal interrupt signal, and

said central processor letting the data stored in said shift register be written into said reception FIFO circuit, when the second interrupt signal is input thereto.